Characterization & Comparative Analysis of High Speed CMOS Comparator for Pipelined ADC

Priyesh P. Gandhi, N. M. Devashryae

Abstract—In today’s high speed low power era, there is an increasing demand of a High Speed Comparator for ADC, DAC and various other applications in an analog and digital domain. This paper describes and analyzes five different architecture for low power and high speed comparators. In this paper, authors have analyzed and simulated the designs using TSMC 0.35 m CMOS technology with 2.0V for preamplifier based comparator and 1.8V power supply for dynamic comparators. The simulation results allow the circuit designer to fully explore the tradeoffs in comparator design, such as offset voltage, speed, power and area for Pipelined A/D Converters. Prelayout and postlayout simulations are carried out using Eldo SPICE tool and layout using IC Station.

Index Terms—Analog to Digital Converters, CMOS, Comparators, Offset, Propagation Delay

I. INTRODUCTION

The rapidly growing market of portable electronic systems such as wireless communication devices, consumer electronics or battery-powered medical devices increases the demand for developing low voltage and low-power circuit techniques and building blocks [1]. In today’s world, where demand for portable battery operated devices is increasing, a major thrust is given towards low power methodologies for high resolution and high speed applications. One such application where low power, high resolution and high speed are required is Analog-to-Digital Converters (ADCs). In the past, pre-amplifier based and differential comparators have been used for ADC architectures. The main drawback of pre-amplifier based comparators is the high constant power consumption. Dynamic comparators are widely used in the high speed ADCs due to its low power consumption and fast speed.

II. PREAMPLIFIER BASED COMPARATOR

The comparator consists of three stages; the input preamplifier, a positive feedback or decision stage, and an output buffer. Differential amplifier will act as a preamplifier circuit. Higher gain can be obtained if the size of M3 and M4 is larger than the size of M31 and M41[2]. Latch stage is also called decision circuit and capable of discriminating mV difference in the logic level. A self biasing differential amplifier is used as the comparator output buffer. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal. Current Mirror is used in the design for providing a constant current over a wide range of voltage [2]-[3].
Fig. 3. Propagation Delay Preamplifier based Comparator

Fig. 4. Frequency Response of Preamplifier based Comparator

Fig. 5. Layout of Preamplifier based Comparator

Fig. 6. Offset of Preamplifier based Comparator

Fig. 7. Propagation Delay Preamplifier based Comparator

Fig. 8. Frequency Response of Preamplifier based Comparator

B. Layout and Postlayout Simulation Results
III. DIFFERENTIAL COMPARATOR

A fully differential typical dynamic comparator is shown in Fig. 9 [4]. The comparator consists of two cross coupled differential pairs with inverter latch at the top. Comparison is made based on the inverter currents, which are related to the inputs, when the clk goes high [4], [5]. The transistors connected to the input and reference (M1M4) are in the triode region and act like voltage controlled resistors. If no mismatch is present the comparator changes its output when the conductances of the left and right input branches are equal $g_L = g_R$. By denoting $W_A = W_4$ and $W_5$ and $W_B = W_2 = W_3$ the input voltage where the comparator changes the state is

$$V_{in+} - V_{in-} = \frac{W_B}{W_A} (V_{ref+} - V_{ref-})$$

The transconductance of the transistors M1M4 operating in the linear region can be approximately written

$$g_{m1,2,3,4} = \mu_0 C_\text{ox} \frac{W_{1,2,3,4}}{L} V_{ds1,2,3,4}$$

A. Prelayout Simulation Results

Fig. 10. Offset of Differential Comparator

Fig. 11. Transient Response (Propagation Delay) of Differential Comparator

Fig. 12. Frequency Response (Gain) of Differential Comparator
B. Layout and Postlayout Simulation Results

Fig. 13. Layout of Differential Comparator

Fig. 14. Offset of Differential Comparator

Fig. 15. Transient Response (Propagation Delay) of Differential Comparator

Fig. 16. Frequency Response (Gain) of Differential Comparator

IV. Dynamic Comparator

A dynamic comparator is present in this section which addresses the problems in the differential comparator as shown in Fig. 17 [6]. The first modification is related to the tail current clock signal. Instead of using the same clock as that for the top switches, which goes from $V_{ss}$ to VDD, a same phase restricted voltage swing clock ($\phi_{clk,B}$) has been used, i.e. $\phi_{clk,B}$ high is less than VDD. $V_{in+}$ and $V_{ref+}$ (and $V_{in-}$ and $V_{ref-}$) are combined in one differential pair as compared to $V_{in+}$ and $V_{in-}$ (and $V_{ref+}$ and $V_{ref-})$ [6],[7].
A. Prelayout Simulation Results

Fig. 18. Offset of Dynamic Comparator

Fig. 19. Transient Response (Propagation Delay) of Dynamic Comparator

Fig. 20. Frequency Response (Gain) of Dynamic Comparator.

B. Layout and Postlayout Simulation Results

Fig. 21. Layout of Dynamic Comparator

Fig. 22. Offset of Dynamic Comparator

Fig. 23. Transient Response (Propagation Delay) of Dynamic Comparator
V. Dynamic Comparator using Positive F/B

Dynamic comparator using positive feedback is shown in Fig. 25. The hysteresis can also be accomplished by using internal positive feedback [8]. In this circuit there are two paths of feedback. The first is current-series feedback through the commonsource node of transistors M1 and M4. This feedback path is negative. The second path is the voltage-shunt feedback through the gate-drain connections of transistors M9 and M11. This path of feedback is positive. If the positive-feedback factor is less than the negative-feedback factor, then the overall feedback will be negative and no hysteresis will result [8],[9]. If the positive-feedback factor becomes greater, the overall feedback will be positive, which will give rise to hysteresis in the voltage-transfer curve. As long as the ratio $\beta_{M9}/\beta_{M8}$ is less than one, there is no hysteresis in the transfer function. When this ratio is greater than one, hysteresis will result.
B. Layout and Postlayout Simulation Results

Fig. 29. Layout of Dynamic Comparator using Positive F/B

Fig. 30. Offset of Dynamic Comparator using Positive F/B

Fig. 31. Transient Response of Dynamic Comparator using positive F/B

Fig. 32. Frequency Response (Gain) of Dynamic Comparator using Positive F/B

VI. Dynamic Comparator using Positive F/B & pMOS Switch

The Dynamic Comparator using Positive F/B & pMOS Switch design is shown in Fig.-33 is similar as Dynamic Comparator using Positive F/B shown in Fig.-25 of accept two pMOS Switches are connected to the clock and these two pMOS switches draws more current. So mismatches are reduced. After simulation the offset voltage is 1.40 mV.

Fig. 33. Dynamic Comparator using Positive F/B & pMOS Switch
A. Prelayout Simulation Results

- Fig. 34. Offset of Dynamic Comparator using Positive F/B & PMOS Switch

- Fig. 35. Transient Response of Dynamic Comparator using positive F/B & pMOS Switch

- Fig. 36. Frequency Response (Gain) of Dynamic Comparator using Positive F/B & pMOS Switch

B. Layout and Postlayout Simulation Results

- Fig. 37. Layout of Dynamic Comparator using Positive F/B & pMOS Switch

- Fig. 38. Offset of Dynamic Comparator using Positive F/B & PMOS Switch

- Fig. 39. Transient Response of Dynamic Comparator using positive F/B & pMOS Switch
TABLE I  
CHARACTERIZATION & COMPARATIVE ANALYSIS OF HIGH SPEED CMOS COMPARATOR: PRELAYOUT SIMULATION RESULTS

<table>
<thead>
<tr>
<th>Sr.No.</th>
<th>Type of Comparator</th>
<th>Offset(mV)</th>
<th>Delay(ns)</th>
<th>Speed</th>
<th>Gain(dB)</th>
<th>Power Dissipation(mW)</th>
<th>Power Dissipation(mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Preamplifier Based Comparator</td>
<td>38.77</td>
<td>1.25</td>
<td>800MHz</td>
<td>75</td>
<td>2.3</td>
<td>21.31</td>
</tr>
<tr>
<td>2.</td>
<td>Differential Comparator</td>
<td>42.57</td>
<td>0.75</td>
<td>1.33GHz</td>
<td>76.54</td>
<td>1.87</td>
<td>21.57</td>
</tr>
<tr>
<td>3.</td>
<td>Dynamic Comparator</td>
<td>7.78</td>
<td>0.60</td>
<td>1.66GHz</td>
<td>78.94</td>
<td>2.57</td>
<td>21.73</td>
</tr>
<tr>
<td>4.</td>
<td>Dynamic Comparator Using Positive F/B</td>
<td>4.90</td>
<td>0.5</td>
<td>2.00</td>
<td>72.59</td>
<td>1.97</td>
<td>21.84</td>
</tr>
<tr>
<td>5.</td>
<td>Dynamic Comparator Using Positive F/B &amp; pMOS Switch</td>
<td>1.40</td>
<td>0.45</td>
<td>2.22</td>
<td>74.94</td>
<td>2.37</td>
<td>21.97</td>
</tr>
</tbody>
</table>

TABLE II  
CHARACTERIZATION & COMPARATIVE ANALYSIS OF HIGH SPEED CMOS COMPARATOR: POSTLAYOUT SIMULATION RESULTS

<table>
<thead>
<tr>
<th>Sr.No.</th>
<th>Type of Comparator</th>
<th>Offset(mV)</th>
<th>Delay(ns)</th>
<th>Speed</th>
<th>Gain(dB)</th>
<th>Power Dissipation(mW)</th>
<th>Power Dissipation(mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Preamplifier Based Comparator</td>
<td>45.52mV</td>
<td>1.4</td>
<td>714MHz</td>
<td>49</td>
<td>3.41</td>
<td>31.312</td>
</tr>
<tr>
<td>2.</td>
<td>Differential Comparator</td>
<td>44.10mV</td>
<td>0.78</td>
<td>1.28GHz</td>
<td>74.58</td>
<td>3.65</td>
<td>37.591</td>
</tr>
<tr>
<td>3.</td>
<td>Dynamic Comparator</td>
<td>9.30mV</td>
<td>0.65</td>
<td>1.52GHz</td>
<td>74.44</td>
<td>3.97</td>
<td>39.390</td>
</tr>
<tr>
<td>4.</td>
<td>Dynamic Comparator Using Positive F/B</td>
<td>5.30</td>
<td>0.54</td>
<td>1.85</td>
<td>70.04</td>
<td>2.48</td>
<td>22.400</td>
</tr>
<tr>
<td>5.</td>
<td>Dynamic Comparator Using Positive F/B &amp; pMOS Switch</td>
<td>1.80</td>
<td>0.49</td>
<td>2.02</td>
<td>71.44</td>
<td>2.93</td>
<td>27.024</td>
</tr>
</tbody>
</table>

Fig. 40. Frequency Response (Gain) of Dynamic Comparator using Positive F/B & pMOS Switch

VII. CHARACTERIZATION & COMPARATIVE ANALYSIS

The pre-layout and post-layout simulations are carried out using ELDO Spice and Layout is done using IC-Station Tool from Mentor Graphics. Following Table-I and Table-II shows the comparative analysis of the different architectures of the CMOS Comparator Design which is presented in this thesis. The comparator is characterized in terms of the offset, propagation delay, gain, power dissipation and area. The simulation results allow the circuit designer to fully explore the tradeoffs in comparator design, such as offset voltage, speed, power and area for Pipelined A/D Converters. In the past, Preamplifier Based and Differential Comparators have been used for ADC architectures such as flash and pipeline. The main drawback of pre-amplifier based comparators is the high constant power consumption. Dynamic comparators are widely used in the high speed ADCs due to its low power consumption and High speed. As shown in Table-I and II Dynamic Comparator has low offset, high speed and low power consumption as compared to the Preamplifier Based Comparator and Differential Comparator. By adding Feedback as shown in Fig-27 the Dynamic Comparator which is presented here can be realized for the flash and pipelined A/D Converters because of the less offset, high speed, low power consumption and less area.

VIII. CONCLUSION

The comparators are simulated in TSMC 0.35m standard digital CMOS process. Results are tabulated in Table I and II. We have observed that the dynamic comparator can be realized for the flash and pipelined ADC because it shows low offset, high speed, high gain and low power dissipation compared to preamplifier based comparator and differential comparator. Further by decreasing the number of transistors and scaling of each transistor, less area, low power dissipation and high speed can be achieved.
REFERENCES


Priyesh P. Gandhi received the B.E. Degree in Electronics & Communication Engineering from Govt. Engineering College, Modasa, Hemchandracharya North Gujarat University, Patan in 2004, and the M.Tech degree in VLSI Design form Institute of Technology, Nirma University, Ahmedabad 2010. He is life member of IEEE, New Delhi. He is worked as a Lecturer at Laljibhai Chaturbhai Institute of Technology, Bhandu (Mehsana) Gujarat from 2005 to 2010 & presently working as an Assistant Professor. His current interests include Low Power, low-voltage High Speed VLSI Design.

Dr. N. M. Devashrayee received M. Sc. in Applied Physics from Faculty of Technology & Engineering M. S. University, Vadodara, India. 1977 and Ph. D. Physics, Kurukshetra University, India, 1990. He worked at Central Electronics Research Institute, Pilani as a Scientist for 23 years. Experience includes research and development in Microelectronics area particularly in VLSI, Sensors and Solid State Devices. He was teaching at PG level in Gujarat University, BITS, IITs as a Visiting Faculty to teach complete IC Technology, VLSI Technology and served as an examiner. He also Member of Board of Under Graduate Studies in Electronic Science Department, Kurukshetra University and Electronic Science Department, Gujarat University. He delivered number of lectures on IC Technology at S.P. University, V. V. nagar & Gujarat University for refresher courses. Filed two patents in humidity sensor and radiation harden MOSFET for VLSI. He was recipient of Raman Research Fellowship Award to participate in post-doctorate study program. Presently Dr. Devashrayee is working as a Section Head of Electronics Research Fellowship Award to participate in post-doctorate study program. Presently Dr. Devashrayee is working as a Section Head of Electronics & communication Department, Coordinator VLSI Design Course at PG level & Head of Physics department at Nirma University, Ahmedabad.