Implementation of Low Power Rail-To-Rail Dynamic Latch Comparator With Modified Adaptive Power Control Technique

Vijay Savani and N. M. Devashrayee

***Abstract*—this paper presents a modified technique of power reduction for the preamplifier based dynamic latch comparator. The comparator presented is having a preamplifier followed by dynamic latch topology based comparator. The dynamic latch is consisting of cross coupled inverters to achieve high speed and at a same time, preamplifier helps to reduce kickback effect. Moreover, a modified power control technique is presented to minimize the power consumption. The implemented design is a rail to rail input range and low power, which can be suitably used in low-to-medium speed Analog to Digital converters. Said design is implemented in 90nm technology using HSPICE. The simulation results have shown that the power consumption of comparator is 916.9µw at the clock frequency of 200MHz and 1V supply voltage with a delay of 80.3ps.**

Index Terms – CMOS, Analog-to-Digital convertor, Dynamic Latch Comparator, Adaptive Power Control, VLSI, Low Power.

I. INTRODUCTION

Over past many years, growing interest for low-power and high speed analog-to-digital converters (ADC) has been a major force driving the semiconductor industry toward increased integration of functional blocks with in a single integrated circuit. Low power electronics devices nowadays are essential in many of the systems like biomedical instruments, mobile devices and others portable battery operated devices. Environment surrounding us being analog in nature while its processing part is in digital domain. So, analog-to-digital converters (ADCs) play vital role in conversion of data from one domain to the other [9-11]. Small power consumption and less propagation delay are the need of the day and one of the ways to achieve this is technology scaling in terms of channel length. Scaling down the feature size of the transistor is not the straight forward process due to the various fabrication complexities and constrains. Reduction in the feature size tends to reduce the supply voltage which in turn limits the maximum input voltage swing. Component mismatch and random noise are also factors those affect the performance of system. All of above are the main concern for Voltage comparator circuit. The overall performance of ADC is solely depends on the comparator design. The comparator must poses ability to resolve the input difference as fast as possible. Moreover, it should consume less power and should have high sensitivity for good resolution [8], [22-24].

The preamplifier in the design is being used for increasing the signal level and ultimately the resolution. It also helps to reduce the effect of kick-back noise. There are basically two types of latch namely static and dynamic, which can be used in comparators. Dynamic latch based comparator is extensively used in analog and mixed-signal circuits to compare two analog input voltages to generate a binary output. The latch is mainly used, (i) to increase the output voltage level to a valid logic level, (ii) to provide gain and (iii) to increase the decision time and hence the speed. Thanks to its power efficiency, the dynamic latched based comparator is currently the most widely used architecture [12-13], [19-20], [24].

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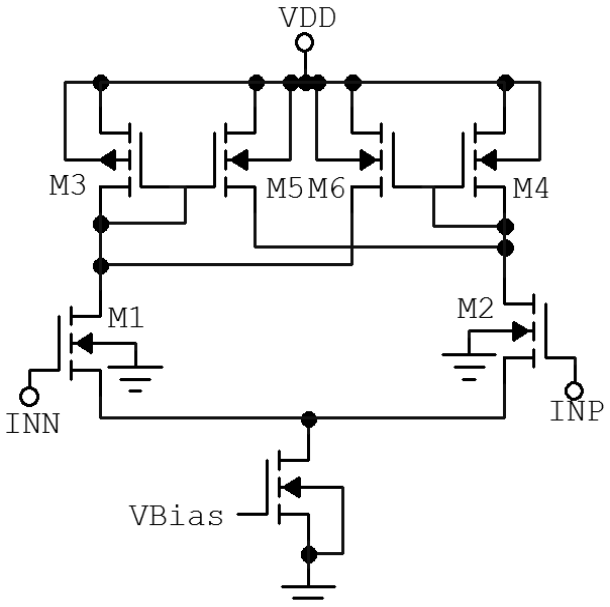

Fig. 1. Conventional Static Latch Comparator

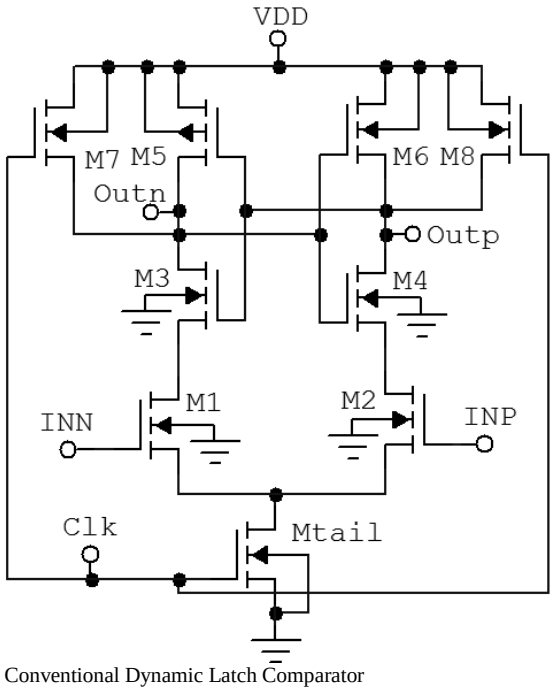

Fig. 2. Conventional Dynamic Latch Comparator

The schematic diagram of conventional static latch comparator and dynamic latch comparator is shown in the Fig. 1 and Fig. 2 respectively [3-5], [7] [17]. In static latch comparator, there is no clock/switch so its power consumption is high compared to the counterpart i.e. dynamic comparator, which possess the clock/switch. In dynamic comparator, when the clk is at low level, the comparator is said to be in reset state and the outputs are reset to Vdd. When the clk signal changes to high logic level, evaluation/regeneration state starts and cross coupled inverter forces one of the output node to ground and other to attain Vdd, depending on the input signal values. Because of the abrupt changes at output, spike will be generated at the drain of input transistor, which is normally referred as a kick back noise [6], [14-16]. Static latch based comparator is not suffering from this phenomena, but the power consumption is larger in the static latch comparator.

During regeneration phase the conventional preamplifier based dynamic comparator consumes power and that would be during half of the clock cycle. Once the decision is being taken place, if these preamplifier is made turned off during the regeneration phase, instead of during entire half period then the power efficiency will increase with reduced power consumption.

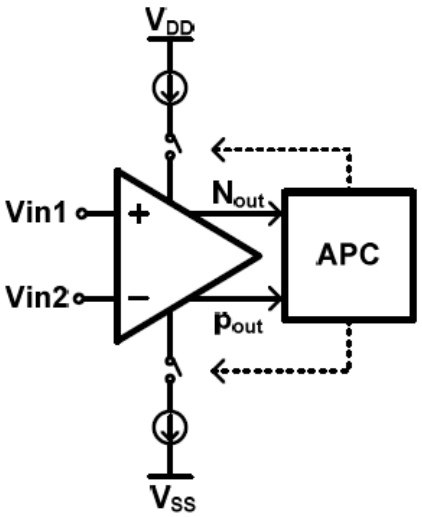

Fig. 3. Adaptive power reduction concept controlled by APC

Fig. 3 shows the technique of power reduction called Adaptive Power Control (APC) [7], [17]. The APC circuit will detect the valid output and generate the control signal i.e. APC signal to turn off the preamplifier section as soon as the decision takes place and reduces the power.

In this paper, a modified adaptive power control technique (APC) is presented and compared with the existing adaptive power control topologies along with existing comparator topology of ref [5] [18]. The presented comparator basically consists of PMOS type and NMOS type differential pairs as a preamplifier followed by a dynamic latch to enhance the decision making speed. A modification in the adaptive (dynamic) power control circuit topology is proposed, which is used to reduce the power consumption with the power efficiency of 98.41%.

Rest of this paper is organized as follows: Section II gives idea about previous two comparator architectures and different power reduction circuit topologies. The proposed modified adaptive power reduction circuit topology is discussed in the Section III. Simulation results are described in Section IV. Finally, conclusion is drawn in Section V.

II. Rail-to-Rail Comparators Topologies

The static latch based comparator has more power consumption then the dynamic latch based comparator, as it suffers from the static current flow during the entire operation. The basic circuit topology of static latch based comparator is shown in Fig. 1. Not only power inefficiency, but it also suffers from some other drawbacks like limited input range (Vth to Vdd) and the kick-back noise [3], [5-7].

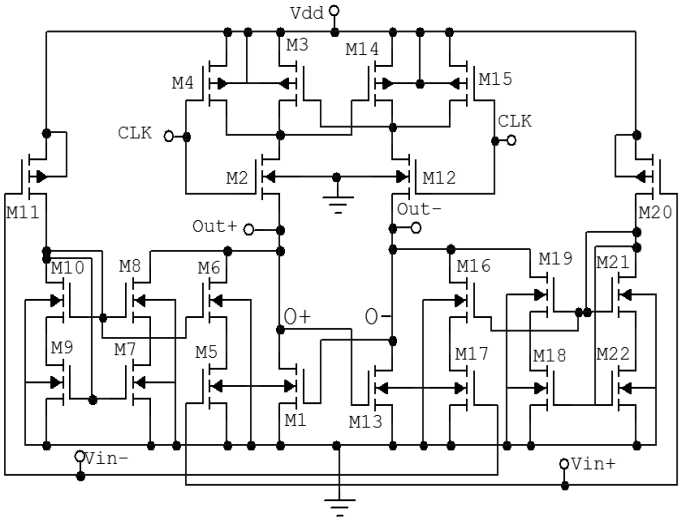

Fig. 4. Schematic of comparator

Preamplifier and latch based comparator schematic is shown in the Fig. 4 [21]. There is no switch available in the preamplifier section of the comparator. The voltage variation at the drain of input transistor is small compared to the topology that have switch in preamplifier section, which results in low kick-back noise. On the other hand, no switch in amplifier section results into more power consumption. As mentioned earlier, Adaptive Power Control Circuit (APC) can help reducing the power consumption.

Two different structures of the preamplifier and dynamic latch based comparator are discussed in following sub sections and the comparator topology of ref [5], [17] is being used with modified adaptive power control technique for implementation in this paper.

A. Rail-to-Rail coparator With adaptive power control using D flip-flop

The rail-to-rail comparator topology and the APC configuration circuit are shown in the Fig. 5 and Fig. 6 respectively [7] [18]. Basically, adaptive power control (APC) blocks cut off the DC power supply of the comparator configuration once the decision is made (completed) in evaluation phase. It avoids the static current flow in the circuit and ultimately helps to reduce overall power consumption [7], [18].

The good parts of this comparator topology is that as there is no reset transistor switch in the preamplifier stage, the voltage swing at the drain of the input differential transistor is very small and the configuration has less kick back noise [7]. Even though

this APC cuts off the DC supply in the first stage of comparator i.e. preamplifier, there are some drawbacks of the topology. One of them is, the large amount of leakage current flows in the second stage i.e. dynamic latch and output buffer during the reset phase. Other is, output terminals O+ and O- are settled down to the potential in between Vdd and ground, which floats the transistors (i.e. P5-P8) and hence the output buffer cannot be fully turned off during reset phase. Because of mentioned phenomena there is a large leakage current, which flows in the latch stage adds more power consumption and ultimately overall power consumption of the comparator increases.

Apart from these problems, the second issue is related to the APC circuit. The APC block helps reducing power consumption in the preamplifier stage, but the APC block itself is very complex, requires more MOS transistors and consumes more power.

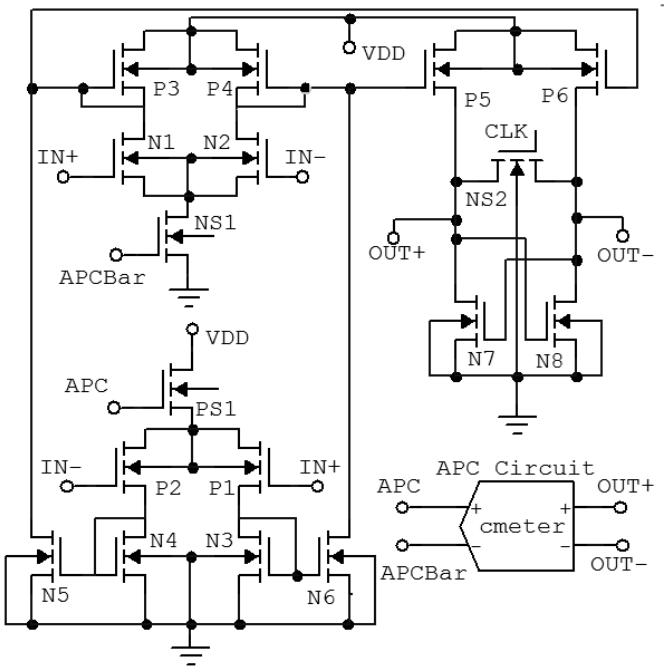

Fig. 5. Schematic of rail-to-rail comparator

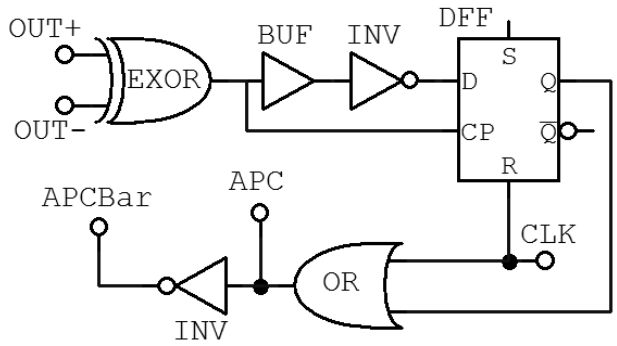

Fig. 6. Adaptive Power Control topology using D Flip-Flop

B. *Rail-to-Rail comparator With adaptive power control using two Ex-Or gates*

The circuit configuration of the modified rail-to-rail comparator is shown in the Fig. 7 [5]. The new APC topology using two EXOR gate is shown in the Fig. 8 [5]. In the circuit topology of Fig. 7, transistors N1, N2, N3, N4 and P1, P2, P3, P4 make first stage i.e. the preamplifier. Transistors P5, P6, N7, N8 form the second stage i.e. dynamic latch stage. Transistors N1, N2, P1 and P2 form input differential amplifier configuration having rail-to-rail input range.

When the clk is at low value, the circuit is in the first half (reset phase) and transistors N5-6, NS1-2 are turned off and the transistors (reset transistors) P7 and P8 are switched on. This make sure that there is no static current in reset phase. In the second half (evaluation phase) of the when the clk is high, transistors P7, P8 are turned off and transistors N5-6, NS1-2 are switched on. Differential pair and the latch stages are in conduction mode at starting of evaluation phase. The input differential voltage is converted in to the equivalent differential current and it is being mirrored to the regenerative dynamic latch stage. Thanks to the strong positive feedback of the latch, which makes it possible to regenerate the small input differential voltage into a full swing output voltage.

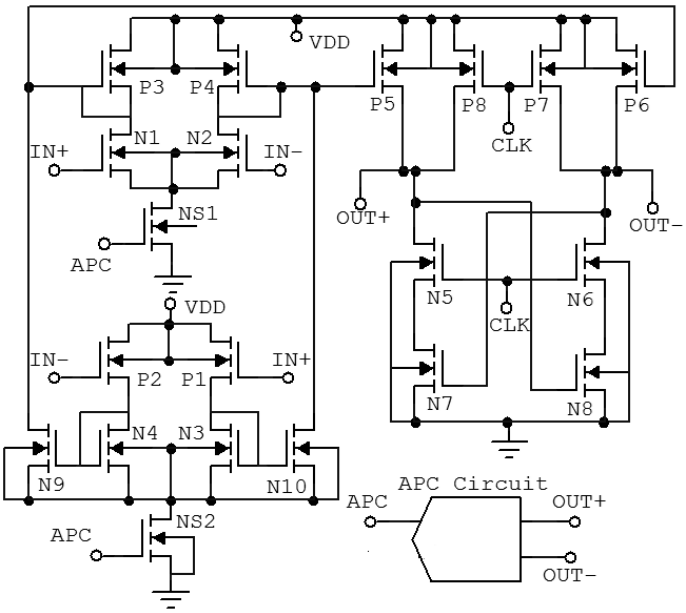

Fig. 7. Modified rail-to-rail comparator

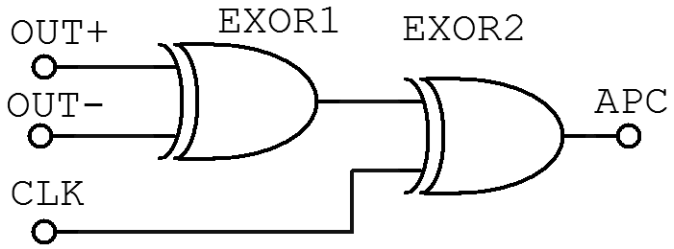

Fig. 8. Schematic APC topology using two XOR gates

After the evaluation is being taken place, output triggers adaptive power control block. When clk is at low logic level (the circuit is in the reset phase), output nodes O+ and O- are pulled to Vdd by means of reset transistors P7-P8 and hence, the output of EXOR1 gate is low. In this mode the output of the EXOR2 gate follows the input clk. The moment the clk is changed from low (‘0’) to high (‘1’), APC signal also changes to high logic level. As APC signal is high, the preamplifier stage turns on from off. After the evaluation is being taken place, one of the output node becomes Vdd and other becomes ground and output of XOR1 becomes high. After these, the APC signal turns into low state because both the input terminals of the XOR2 are high.

Once the APC signal becomes low, it turns off the DC supply of the preamplifier. The various signal states of outputs, clock and the APC signal under various conditions are shown in Table I.

TABLE I
SIGNAL STATE OF VARIOUS TERMINALS

Clk	Output+	Output-	APC	State
0	1	1	Clk	Reset
0 to 1	0	1	0 to 1 to 0	Evaluated
0 to 1	1	0	0 to 1 to 0	Evaluated

The simulated waveforms of the Adaptive Power Control signal is shown in Fig. 9. There are two APC signals being generated during each clock cycle, one is during evaluation phase and another during the reset phase. The width of the APC pulse during the reset phase is of short duration, because the output nodes are reset to Vdd during reset phase by two PMOS transistors P7-P8. Second APC signal is generated at beginning of the falling edge of the Clk. This APC signal has very short duration span and magnitude, as a result the power added by this second pulse is very small. Furthermore, this second pulse can also be removed by adding extra logic circuitry into the APC block, but the power added by this extra logic compensated by not adding it into the circuit.

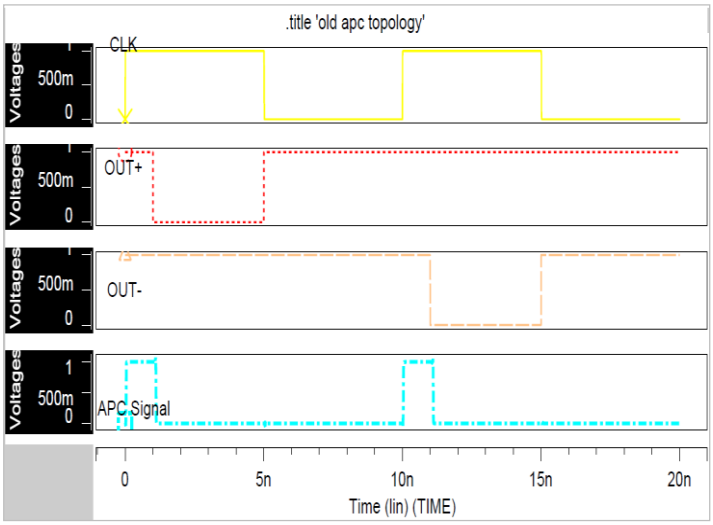

Fig. 9. Simulated Waveform of APC signal

III. THE COMPARATOR WITH PROPOSED MODIFIED ADAPTIVE POWER CONTROL CIRCUIT

For the implementation and verification of modified Adaptive Power Control topology, the circuit topology shown in Fig. 7 is used as a comparator. Fig. 10 shows the configuration of modified APC block. The APC circuit is implemented using only one NAND gate and one inverter.

The functionality of the modified APC block is as follow: After the evaluation is being done, output triggers adaptive power control block. In the reset phase, clock is low and the output terminals are being pulled to Vdd by the reset transistors and as a result, output of NAND gate is HIGH. Evaluation phase begins when the clock becomes high. As the clock is changing from low to high the output of NAND gate becomes LOW. Moment the evaluation is being done, one output terminal is at Vdd and other is at Ground, as a result the output of the NAND gate turns into HIGH state. Though the DC power supply controlling switches in the preamplifier is NMOS device, the output of the NAND gate is inverted to get the final APC signal, which becomes input to the transistors NS1 and NS2.

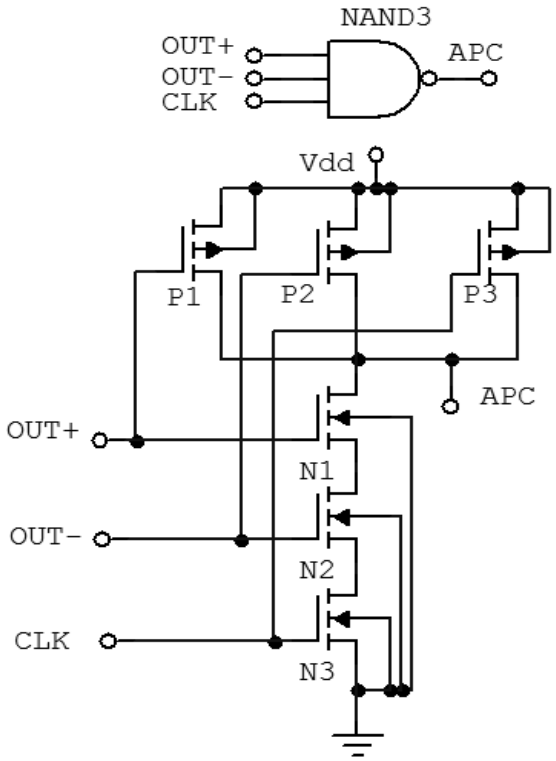

Fig. 10. Modified Adaptive Power Control topology

The signal state of various terminals i.e. output, clock, APC signal and APC' signal under various conditions are shown in Table I.

TABLE II
SIGNAL STATE OF VARIOUS TERMINALS

Clk	Out put +	Out put -	APC	APC'	State
0	1	1	1	0	Reset
0 to 1	1	0	1 to 0 to 1	0 to 1 to 0	Evaluated
0 to 1	0	1	1 to 0 to 1	0 to 1 to 0	Evaluated

Table III shows the comparison of the total no. of required MOS transistors and power consumption of ref [5] and modified APC block with modified rail-to-rail comparator. Simulation result shows that the power consumption of the APC block is 789.67µW in case of the APC block of ref [5] whereas for the modified APC block it is 131.60µW. Result shows that the significant reduction in the power consumption is achieved by APC block.

TABLE III
COMPARISON OF APC [5] AND MODIFIED APC

APC Configuration	No of MOS transistor	Power Consumption (APC Block only)
APC Ref [5]	32	789.67 µW
Modified APC	8	131.60 µW

IV. SIMULATION RESULTS

Fig. 11 shows the simulation results of APC signal of modified APC block and the Fig. 12 shows the transient simulation results of complete configuration.

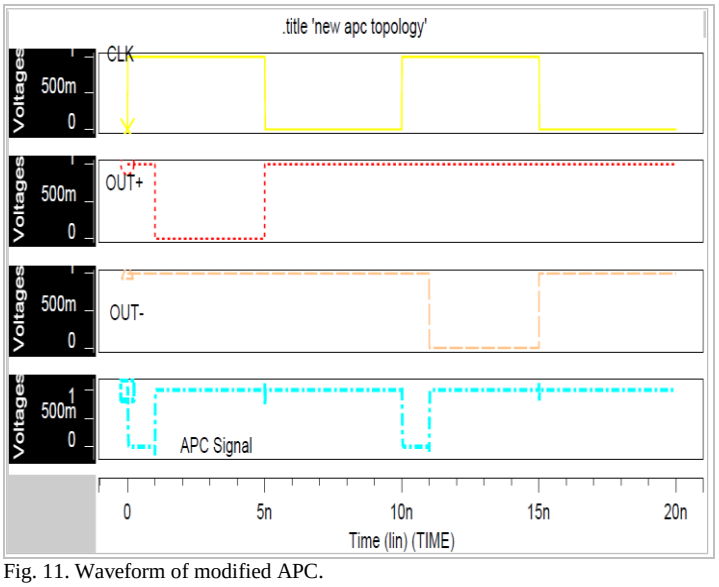

Fig. 11. Waveform of modified APC.

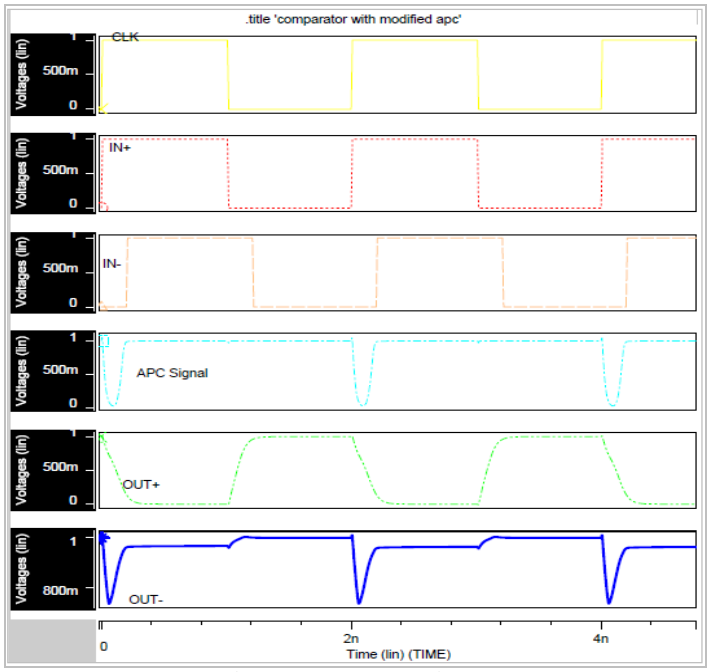

Fig. 12. Transient results of comparator with modified APC

The comparator with modified APC block is implemented in 90nm CMOS technology. The power consumption of the proposed configuration is 916.9µW at a frequency of 200MHz. The simulation results of power and delay are summarized in Table IV. Comparing the proposed structure with [5], [7] and [17], there is no static current flowing in the circuit and in addition to this, the adaptive power control circuit structure is much simpler, which gives rise to the lowest total power consumption amongst all these three circuits. Table summarizes the power consumption and delay of comparator [5], [17] without APC, comparator with APC block [5], [17] and comparator with modified APC block.

TABLE IV
POWER AND DELAY COMPARISON

Parameter	**Comparator (Without APC)**	**Comparator With (OLD APC)**	**Comparator With (Modified APC)**
Power (mW)	57.8	6.21	**0.9169**
Delay (ps)	96.67	52.19	**80.3**
Technology=90nm, Supply Voltage=1V, Clock Frequency=200MHz, C_L=0.005pF			

The efficiency in terms of power-reduction can be expressed by means of Equation (1). In the equation $P_{withoutAPC}$ is the power dissipation of the comparator without APC block whereas $P_{withAPC}$ is the power dissipation of the comparator with APC block. Based on this formula the power efficiency of comparator [5] with old topology of APC block and with modified APC block is calculated and summarize in Table V.

$$\eta = 1 - {}^{P_{WithAPC}}/_{P_{withoutAPC}} \qquad (1)$$

TABLE V
POWER EFFICIENCY COMPARISON

Power Efficiency (OLD APC)	**Power Efficiency (Modified APC)**
89.25 %	98.41 %

V. CONCLUSION

The modified structure of the Adaptive Power Control structure is discussed. Existing topologies of APC block is compared with the proposed APC block and the power efficiency has been derived. The power efficiency of the comparator with existing APC block [5] [17] is 89.25%, whereas with the help of modified structure of APC block it has been increased to 98.41%. The proposed APC block can be used with comparator having preamplifier, to reduce the total power consumption of the circuit. The proposed structure consumes only 916.9µW at a frequency of 200MHz and delay of 80.3ps having 1V power supply.

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